SEEQC, INC.

SUPERCONDUCTING QUANTUM CONTROL CIRCUIT ELECTRONICS FABRICATION PROCESS

PROCESS #QC1000A

DESIGN RULES

REVISION #5, JUL 13, 2021

Direct all inquiries, questions, comments and suggestions concerning these design rules and/or SeeQC fabrication to:

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Preface

SeeQC, Inc. has developed and sustains several fabrication processes for superconductor electronics. This document specifies the design rules of SeeQC fabrication process #QC1000A for niobium-based superconducting integrated circuits. This information constitutes a self-contained guide to the physical layout of devices and circuits within the scope of the standard SeeQC fabrication process. Adherence to these rules will provide cost-effective, high-yield designs.

1.0 General Description

1.1 This SeeQC IC fabrication process uses only refractory materials, with the exception for a Pd/Au metallization layer used for contact pads. Niobium is used as the superconducting material due to its comparably high critical temperature, electrical and thermal stability, and ability to be thermally cycled many times without degradation. Niobium/Aluminum-Oxide/Niobium Josephson tunnel junctions are made by depositing an *in-situ* trilayer across the entire wafer and subsequently defining junction areas by deep-UV photolithography and etching. This method yields good uniformity and reproducibility of junction parameters.

1.2 The critical current density of $Nb/AlO_x/Nb$ trilayer associated with QC1000A is 1 kA/cm^2 (10 $\mu A/\mu m^2$).

1.3 The Josephson junctions can be interconnected into circuit configurations using four superconducting layers: junction base electrode (layer M1), two Nb wiring layers (layers M2 and M3), superconducting Nb ground plane (layer M0) and a NbNx high kinetic inductance layer below the ground plane (MN1)

1.4 The sheet resistance of the resistive layer (R2) is a Ti/PdAu/Ti resistive material with sheet resistance of 4.0 ohms/sq and a thickness of 40±10 nm.

1.5 Low loss SiNx is used is deposited to provide insulation between the conducting layers. Anodization of the base electrode of trilayer provides additional insulation to Josephson junctions.

1.6 QC1000A is fabricated on a 150-mm diameter (6-inch) high resistivity Si wafers.

#	Layer	GDS#	Mask polarity	Description
				Al/NbNx deposition
1	MN1	34	+	MN1 layer patterning
				Low loss SiN_x deposition
2	IN1	32	-	Contact (via) between MN1 and M0 patterning
				Nb deposition
3	M0	30	-	M0 patterning (holes in niobium ground plane)
				Low loss SiN_x deposition
				CMP “Caldera” planarization
4	I0	31	-	Contact (via) between M1 and ground plane patterning
				$Nb/Al/AlO_x/Nb$ trilayer deposition (see 1.2)
5	J1	4	+	Counter-electrode (junction area) definition
				Base electrode anodization
6	A1	5	+	Anodization layer patterning
7	M1	1	+	Trilayer base electrode patterning
				Low loss SiN_x deposition
8	R2	9	+	Resistive layer patterning
				Resistive layer deposition (see 1.4)
				Low loss SiN_x deposition
9	I1	3	-	Contact (via) between M2 and (J1, R2, or M1)
				Nb deposition
10	M2	6	+	M2 layer patterning
				Low loss SiN_x deposition
11	I2	8	-	Contact (via) between M2 and M3
				Nb deposition
12	M3	10	+	M3 layer patterning
13	I3	13	-	I3 (Dielectric removal from Qubit interface) patterning
14	R3	11	+	Contact pad patterning
				Pd/Au contact metallization deposition
15	BMP-Cu	12	+	“bump” layer for MCM, Copper
16	BMP-In	15	+	“bump” layer for MCM, Indium

Layout Design Rules

2.1 **Minimal** size, spacing, and surround for each layer are specified in the following table:

#	Layer	Rule	µ	Comment
1	**MN1**	***Positive***		**MN1 high-kinetic-inductance wiring layer**
	1.1	MN1 minimal size	0.8	If exact width is required, we recommend using **1.4 um** as a minimal feature.
	1.2	MN1 minimal spacing	1.0	
	1.3	MN1 surround IN1	0.3	
2	**IN1**	***Negative***		**Contact (via) between MN1 and M0**
	2.1	IN1 minimal size	1.0	
	2.2	IN1 surrounded by MN1	0.3	
	2.3	IN1 spacing to M0	0.3	A via should always be covered with metal. M0 is a negative layer, - "spacing" instead of "surrounded by"
	2.4	IN1 edge spacing to J1	0.5	Crossing IN1 pattern with JJs is possible but not recommended
3	**M0**	***Negative***		**Holes in ground plane**
	3.1	M0 minimal size	0.5	
	3.2	M0 minimal spacing	0.5	
	3.3	M0 spacing to I0	0.3	A hole in insulation should always be over metal. M0 is a negative layer, - so, the rule is "spacing to".
4	**I0**	***Negative***		**Contact (via) between M1 and ground plane**
	4.1	I0 minimal size	1.0	
	4.2	I0 spacing to J1	1.0	J1 patterns should not overlap with I0 patterns.
	4.3	I0 surrounded by M1	0.3	A hole in insulation layer must be completely covered by two adjacent metal layers (from top and bottom)
	4.4	I0 edge spacing to R2	0.3	
5	**J1**	***Positive***		**Trilayer counter electrode (junction area) definition**
	5.1	J1 minimal size	0.6	
	5.2	J1 minimal spacing	1.0	
	5.3	J1 surrounded by A1	0.5	A JJ must be covered by anodization layer
	5.4	J1 surrounded by M1	1.0	
	5.5	M0 edge spacing to J1	0.5	
	5.6	I0 edge spacing to J1	1.0	J1 patterns should not overlap with I0 patterns.
	5.7	IN1 edge spacing to J1	0.5	Crossing J1 patterns with IN1 is not recommended.
6	**A1**	***Positive***		**M1 anodization layer patterning**
	6.1	A1 minimal size	1.0	
	6.2	A1 surrounded by M1	0.3	
	6.3	A1 edge spacing to R2	0.3	
	6.4	A1 edge spacing to I1	0.5	I1 surrounded by A1 has no galvanic contact to M1 (only to a JJ)
7	**M1**	***Positive***		**Trilayer base electrode patterning**
	7.1	M1 minimal size	0.8	
	7.2	M1 minimal spacing	1.0	
	7.3	M1 edge spacing to R2	0.3	
	7.4	M1 surround I1 (7)	0.5	

8	**R2**	***Positive***		**Resistive layer patterning**
	8.1	R2 minimal size	0.8	
	8.2	R2 minimal spacing	1.0	
	8.3	R2 surround I1	0.5	A simultaneous contact to both R2 and M1 layers is possible. The overlap area of I1 hole with each layer (R2 and M1) should satisfy rule 8.1
	8.4	M1, I0, or A1 edge spacing to R2	0.3	R2 pattern may not cover any steps (like in I0, A1 or M1). Placing R2 object inside I0, A1 or M1 area is allowed.
9	**I1**	***Negative***		**Contact (via) between M2 and (J1, R2, or M1)**
	9.1	I1 minimal size	1.0	
	9.2	I1 surrounded by M2	0.5	
10	**M2**	***Positive***		**M2 wiring layer**
	10.1	M2 minimal size	0.8	
	10.2	M2 minimal spacing	1.0	
	10.3	M2 surround I2	0.5	
11	**I2**	***Negative***		**Contact (via) between M2 and M3**
	11.1	I2 minimal size	1.8	
	11.2	I2 surrounded by M3	0.5	
12	**M3**	***Positive***		**M3 wiring layer**
	12.1	M3 minimal size	2.0	
	12.2	M3 minimal spacing	2.0	
	12.3	M3 minimal contact with R3	5.0	R3 layer is deposited directly on M3 (without insulation). To provide a reliable electrical contact between objects in R3 and M3 layers, the overlap should be no less than 5 micron.
13	**I3**	***Negative***		**Di-electric removal from selected area**
	13.1	I3 minimal size	1.8	
	13.2	I2 surrounded by M3	0.5	
14	**R3**	***Negative***		**Pd/Au contact metallization**
	14.1	R3 minimal size	5.0	
	14.2	R3 minimal spacing	3.0	
	14.3	R3 surrounded by M3	0.5	
15	**BMP1**	***Negative***		**Copper bumps layer for MCM**
	15.1	BMP1 minimal size	10	
	15.2	BMP1 minimal spacing	30	
16	**BMP2**	***Negative***		**Indium bumps layer for MCM**
	16.1	BMP2 minimal size	15	
	16.2	BMP2 minimal spacing	30	
	16.3	BMP2 surround BMP1	2.5	

3.0 Physical Layer Process Specifications

3.1 Since the fabrication process involves projection photolithography and etching, the size of features (e.g., linewidth) on the wafer may systematically differ somewhat from the designed feature size. This change in size is called "bias". In the table below, the bias is defined as the shift of the object's edge due to its enlargement/reduction relative to its intended position in the design. It is often called single-side bias. A positive bias means that the digitized areas become larger on the wafer than in the design. The biases shown below for all layers, except J1, are applicable to relatively extended objects with sizes larger that the minimal feature size for a given layer. In most cases, sharp corners will be rounded up.

Layer	Material	Bias (3.1) μm	Physical layer properties: resistance, capacitance, *etc*.	Thickness nm
MN1	NbN_x	0.0±0.1	Nb, superconductor. Penetration depth λ_L = 450 nm ± 20 nm	40±4
IN1	SiN_x	0.0±0.1	SiN_x, insulator. Capacitance: 0.66 fF/μm^2 ± 20%	100±10
M0	Nb	0.0±0.1	Nb, superconductor. Penetration depth λ_L = 90 nm ± 10 nm	200±10
I0	SiN_x	0.0±0.1	SiN_x, insulator. Capacitance: 0.44 fF/μm^2 ± 10%	150±15
M1	Nb	0.0±0.1	Trilayer base electrode, superconductor. λ_L = 90 nm ± 10 nm	135±10
J1	Nb	0.0±0.02	Josephson tunnel junction counter electrode (see 3.2 and 3.3)	50±5
A1	Nb_2O_5/Al_2O_3	0.0±0.1	Layer of the anodized surface of base electrode (i.e., surrounding a Josephson junction). Capacitance: 5.0 fF/μm^2 ± 20%	40±5
	SiN_x		SiN_x, insulator. Capacitance: 0.66 fF/μm^2 ± 10%	100±10
R2	Mo	0.0 ± 0.1	4.0±0.2 Ohm per square	40±6
	SiN_x		SiN_x, insulator. Capacitance: 0.66 fF/μm^2 ± 10%	100±10
I1		0.0 ± 0.1	Contact hole through the above two SiO_2 layers	
M2	Nb	-0.1 ± 0.05	Nb, superconductor. Penetration depth λ_L = 85 nm ± 5 nm	300±20
	SiN_x		SiN_x insulator. Capacitance: 0.13 fF/μm^2 ± 10%	500±40
I2		0.0 ± 0.1	Contact hole through the above insulator	
M3	Nb/Ta	-0.3 ± 0.1	Nb, superconductor. Penetration depth: λ_L = 85 nm ± 5 nm.	500/100±50
R3	Pd/Au	0.0 ± 1.0	Contact pads metallization	350±60
BMP-Cu	Cu/Au	0.0 ± 1.0	Copper Layer for MCM bump	6000±600
BMP-In	NbNx/In	0.0 ± 1.0	Indium Layer for MCM bump	3000±300

3.2 We recommend using Josephson junctions of **circular** shape. The deviation of the radius of the circle in J1 layer is within +/- 20 nm. If such a deviation is critical, - use "digitized circular shape", i.e. a polygon with vertices of 135 degrees placed on 20-nm grid.

3.3 C_s is the specific capacitance in fF/μm^2 and j_c is the critical current density in μA/μm^2, and plasma voltage in mV.

J_c (μA/μm^2)	0.3	1.0	10.0	45.0	100.0	200.0
C_s (fF/μm^2)	37	40	50	59	65	71
V_p (μV)	52	91	257	501	711	962

3.4 The critical current per micron width for supercoducting films is given in the following table

Layer	MN1	M0	M1	M2	M3
I_c (mA/μm)	2.5	20.0	30.0	50.0	70.0

If the wire crosses steps, its I_c may drop by more than 50%. Please, see the minimal width of a wire in table 2.1 and its bias in table 3.0 before designing current transmitting lines.

3.5 The sheet inductance of the superconducting films is given in the following table

Layer	MN1	M0-M1-M3	M0-M2-M3	M0-M2
Ls (pH/sq)	8.50	0.40	0.38	0.63

3.6 The optional choice of NbN_x for M3 material is available, as well as the Ta deposition.

4.0 Lithography features

4.1 Mask Grid Size

Layer	Polarity	Grid Size [μ]
MN1	Clear field	0.1
IN1	Dark field	0.1
M0	Dark field	0.1
I0	Dark field	0.1
M1	Clear field	0.1
J1	Clear field	0.02
A1	Clear field	0.1
R2	Dark field	0.1
I1	Dark field	0.1
M2	Clear field	0.1
I2	Dark field	0.1
M3	Clear field	0.1
I3	Dark field	0.1
R3	Dark field	0.1
BMP-Cu	Dark field	0.1
BMP-In	Dark field	0.1

4.2 Layer J1 have grid size of 20 nm. All remaining layers must use grid size of 100 nm. Every pixel's coordinates on the mask are being rounded up to the grid.

4.3 All layouts will be printed on wafers as you see them on your computer screen (no mirroring).

5.0 Designs Submission Formats

5.1 The format of layout file is GDS-II.

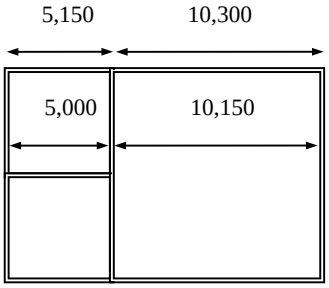
5.2 Please submit designs to SeeQC through File Transfer Protocol (FTP) or, if the size of the file is **less than 10 MB**, via E-mail to customer@seeqc.com

5.3 The active chip area for the design is limited to 5,000 μm x 5,000 μm. On the wafer, it will be surrounded by a dicing channel. Dicing channels between chips are 150 μm wide. No objects are allowed inside a dicing channel (extending beyond the 5,000 μm x 5,000 μm area).

5.4 It is also allowed to submit 1-cm chips. In this case, the design area is 10,150 μm x 10,150 μm. No objects are allowed beyond the 10,150 μm x 10,150 μm area.

5.5 All other sizes should be negotiated with SeeQC prior the submission.

5.6 When delivering layouts of multiple chips to SeeQC, send only **one** GDS file, with all chips placed together in a single "supercell" on a **2,575-μm** grid. A chip insertion point should be at the geometrical center of the chip, i.e. – on the 2,575-μm grid



5.7 No cell (SREF) name may exceed **60 characters**. Cell names will be truncated to this size automatically and might clobber other cells.

5.8 We **do not support** GDS cell (SREF) placements that are rotated by a not multiple of **45 degrees** angle.

6.0 Cycle Time

6.1 Less than 2 months are required to process a wafer.

6.5 Note: fabrication time may vary depending upon customer requirements.

7.0 Miscellaneous

- You must reserve your chip sites at least two weeks prior to the release date.
- Consult SeeQC and obtain an updated quote before submitting layouts.
- If you get permission to update the already-submitted layout, submit the revised layout without changing the names of the parent chips and/or the name of the main cell containing the parent chips. 5mm x 5mm or 10mm x 10mm chips are considered parent chips.
- If you need a layout example, send a request to customer@seeqc.com
    - Layout of a junction defined using anodization.
    - Layout for a simple logic circuit.
    - Layout of a master cell.
- If you use logos or structures in your layouts that are not part of active circuits, make sure that they also follow design rules. We will reject layouts that contain excessive design rule violations.
- Do not “flatten” your chips, - we add specific prefixes to all cell names to prevent name conflicts.
- We fabricate and deliver from 4 to 16 copies of your chips (depending on reticle placement). Should you need specific number of copies, - please contact SeeQC prior the release.