NIOBIUM INTEGRATED CIRCUIT FABRICATION

PROCESS #S1

DESIGN RULES

REVISION #1, NOVEMBER 25, 2019

Direct all inquiries, questions, comments and suggestions concerning these design rules and/or Seeqc fabrication to: foundry@seeqc.com

Preface

Seeqc, Inc. offers to its customers several fabrication processes for superconductor electronics. This document specifies the design rules of Seeqc fabrication process #S1 for niobium-based superconducting integrated circuits. This information constitutes a self-contained guide to the physical layout of devices and circuits within the scope of the standard Seeqc fabrication process. Adherence to these rules will provide cost-effective, high-yield designs.

1.0 General Description

1.1 This Seeqc IC fabrication process uses only refractory materials, with the exception of a Pd/Au metallization layer used for contact pads. Niobium is used as the superconducting material due to its comparably high critical temperature, electrical and thermal stability, and ability to be thermally cycled many times without degradation. Niobium/Aluminum-Oxide/Niobium Josephson tunnel junctions are made by depositing an *in-situ* trilayer across the entire wafer and subsequently defining junction areas by deep-UV photolithography and etching. This method yields good uniformity and reproducibility of junction parameters.

1.2 Seeqc currently offers processes with wide range of critical current densities of $Nb/AlO_x/Nb$ trilayer: 30 A/cm^2 (0.3 μA/μm^2), 100 A/cm^2 (1.0 μA/μm^2), 1 kA/cm^2 (10 μA/μm^2), 4.5 kA/cm^2 (45 μA/μm^2), 10 kA/cm^2 (100 μA/μm^2) and 20 kA/cm^2 (200 μA/μm^2). 30-A/cm^2 and 1-kA/cm^2 critical current densities are available upon request only. The last three densities (4.5, 10 and 20 kA/cm^2) may coexist in one design. The customer must use different JJ definition layers for different J_c (J1/J2/J3 correspondingly).

1.3 Currently, there are four basic superconductor wiring layers: junction base electrode (layer M1), two Nb wiring layers (layers M2 and M3), and Nb ground plane (layer M0). For the reference, this basic process is called a 4-layer process.

1.4 In addition to (1.3), Seeqc provides two superconductor planarized layers (MN1 and MN2) placed below M0 (a 6-layer process). These layers can be used for complex wiring and dc power distribution. These layers are optional and do not have to be present in the design. The number of additional planarized layers is customizable.

1.5 The sheet resistance of the resistive layer (R2) varies for different processes. We use non-superconductive materials for low-temperature oriented processes (30 and 100 A/cm^2). The sheet resistance for low-temperature oriented processes is customizable in the range from 2.0 to 5.0 Ohm/sq.

Process J_c	**Sheet Resistance at 4.2 K, Ohm/□**	**Material**	**T_c, K**	**Thickness, nm**
30 A/cm^2	2.0±0.3	Ti/PdAu/Ti	0.0	100±10
100 A/cm^2	2.0±0.3	Ti/PdAu/Ti	0.0	100±10
1 kA/cm^2	2.0±0.3	Ti/PdAu/Ti	0.0	100±10
4.5 kA/cm^2	2.1±0.3	Mo	0.9	40±6
10 kA/cm^2	3.0±0.3	Mo	0.9	28±6
20 kA/cm^2	4.0±0.5	Ti/PdAu/Ti	1.1	60±6

1.6 Either Silicon dioxide (SiO_2) or Silicon nitride (Si_3N_4) (low-loss) provides insulation between the conducting layers. Anodization of the base electrode of the trilayer provides additional insulation to Josephson junctions.

1.7 Our standard fabrication process uses 150-mm diameter (6-inch) oxidized Si wafers. A process on unoxidized Si, GaAs, or Ge-on-Si wafer is also available upon request. Please inquire Seeqc for pricing info.

1.8 A recently developed high-kinetic inductance layer (HKIL) with 8.5-pH/sq sheet inductance is available upon request in the 4-layer process a 5-th layer (MN1) placed under M0.

1.9 In addition to the contact pad metallization (layer R3), we provide Cu/Au/In bumps for MCM bonding (layer BMP). The height of the bumps is customizable in range from 0.5 to 5.0 μm.

1.10 Seeqc Niobium Process Flow Overview is shown in the table below.

#	Layer	GDS#	Mask polarity	Description
				Nb deposition
1	MN2	38	+	MN2 layer patterning
				SiO_2 or Si_3N_4 deposition
2	IN2	36	-	Contact (via) between MN2 and MN1
				CMP planarization
				Nb deposition
3	MN1	34	+	MN1 layer patterning
				SiO2 or Si3N4 deposition
4	IN1	32	-	Contact (via) between MN1 and M0
				CMP planarization
				Nb deposition
5	M0	30	-	M0 patterning (holes in niobium ground plane)
				SiO2 or Si3N4 deposition
				CMP planarization(1)
6	I0	31	-	Contact (via) between M1 and ground plane
				Nb/Al/AlO_x/Nb trilayer deposition (see 1.2)
7	J1	4	+	Counter-electrode (junction area) definition for 4.5-kA/cm^2 process
7a	J2	21	+	Counter-electrode (junction area) definition for 10-kA/cm^2 process
7b	J3	20	+	Counter-electrode (junction area) definition for 20-kA/cm^2 process
				Base electrode anodization
8	A1	5	+	Anodization layer patterning
9	M1	1	+	Trilayer base electrode patterning
				SiO2 or Si3N4 deposition
				Resistive layer deposition (see 1.4)
10	R2	9	+	Resistive layer patterning
				SiO2 or Si3N4 deposition
11	I1	3	-	Contact (via) between M2 and (J1/J2, R2, or M1)
				Nb deposition
12	M2	6	+	M2 layer patterning
				SiO2 or Si3N4 deposition
13	I2	8	-	Contact (via) between M2 and M3
				Nb deposition
14	M3	10	+	M3 layer patterning
				Pd/Au contact metallization deposition
15	R3	11	+	Contact pad patterning
16	BMP	15	+	“bump” layer for MCM (optional)

1) In the 6-layer process, insulation layers between layers MN2, MN1, M0, and contacts between them (IN2 and IN1) are **planarized**. All other layers are **not planarized**.
2) Insulation on top of layer M0 is **planarized** at the advanced (6-layer) process. At the standard (4-layer, less expensive) process, M0 is **not planarized**.
3) Currently, we **do not support** cell (SREF) placements that are rotated by not **multiple of 90 degrees angle**.
4) In high-Jc (10 and 20-kA/cm^2) designs, Josephson junctions should be defined in layer J2 and J3 correspondingly. JJs for all other critical current densities – in layer J1.

Layout Design Rules

2.1 **Minimal** size, spacing, and surround for each layer are specified in the following table

#	Layer	Rule	µm	Comment
5	**M0**	***Negative*** [(1)]		**Holes in ground plane**
	5.1	M0 minimal size [(2)]	1.0	
	5.2	M0 minimal spacing [(3)]	1.0	
	5.3	M0 spacing to I0[(4)]	0.5	A hole in insulation should always be over metal. M0 is a negative layer, - so, the rule is "spacing to".
	5.4	M0 edge spacing to M1[(5)]	0.3	Lines in M1 may cross M0 pattern in the planarized (6-layer) process without its critical current reduction. In the standard (4-layer) process, crossing M0 with M1 is not recommended.
	5.5	M0 edge spacing to R2	0.3	R2 pattern may cross M0 pattern in the planarized (6-layer) process only.
6	**I0**	***Negative***		**Contact (via) between M1 and ground plane**
	6.1	I0 minimal size	1.0	
	6.2	I0 spacing to J1	1.0	Seeqc cannot guarantee the quality *(e.g., V_m)* and the precise critical current *(I_c)* of a junction residing in I0 hole. Therefore, J1/J2/J3 patterns should not overlap with I0 patterns.
	6.3	I0 surrounded by M1 [(6)]	0.5	A hole in insulation layer must be completely covered by two adjacent metal layers (from top and bottom)
	6.4	I0 edge spacing to R2	0.3	
7	**J1-J3**	***Positive***		**Trilayer counter electrode (junction area) definition**
	7.1	J1 minimal size	0.8	A minimal diameter of a designed JJ. The actual diameter will come out ~0.6µm due to overetch (see3.2).
	7.2	J1 minimal spacing	1.0	
	7.3	J1 surrounded by A1	0.5	A JJ must be covered by anodization layer
	7.4	J1 surrounded by M1	1.0	
	7.5	M0 edge spacing to J1	0.5	
	7.6	I0 edge spacing to J1	1.0	Seeqc cannot guarantee the quality *(e.g., V_m)* and the precise critical current *(I_c)* of a junction residing in I0 hole. Therefore, J1/J2/J3 patterns should not overlap with I0 patterns.
	7.7	IN1 edge spacing to J1	0.5	Crossing J1/ J2/ J3 patterns with IN1 is possible but not recommended.
8	**A1**	***Positive***		**M1 anodization layer patterning**
	8.1	A1 minimal size	1.0	
	8.2	A1 surrounded by M1	0.3	
	8.3	A1 edge spacing to R2	0.3	
	8.4	A1 edge spacing to I1	0.5	If hole in I1 is surrounded by A1, no galvanic contact to M1 is possible (except for via JJ)
9	**M1**	***Positive***		**Trilayer base electrode patterning**
	9.1	M1 minimal size	0.8	
	9.2	M1 minimal spacing	1.0	
	9.3	M1 edge spacing to R2	0.3	
	9.4	M1 surround I1 [(7)]	0.5	
10	**R2**	***Positive***		**Resistive layer patterning**
	10.1	R2 minimal size	0.8	
	10.2	R2 minimal spacing	1.0	
	10.3	R2 surround I1	0.5	A simultaneous contact to both R2 and M1 layers is possible. The overlap area of I1 hole with each layer (R2 and M1) should satisfy rule 11.1
	10.4	M0, M1, I0, or A1 edge spacing to R2	0.3	R2 pattern may not cover steps in I0, A1 or M1 and may cross M0 pattern in the planarized (6-layer) process only. Placing R2 object inside M0, I0, A1 or M1 area is allowed.
11	**I1**	***Negative***		**Contact (via) between M2 and (J1/J2/J3, R2, or M1)**
	11.1	I1 minimal size	1.0	Recommended min. size to J1/2/3 layer is 2.0 um in diameter
	11.2	I1 surrounded by M2	0.5	

12	**M2**	***Positive***		**M2 wiring layer**
	12.1	M2 minimal size	0.8	
	12.2	M2 minimal spacing	1.0	
	12.3	M2 surround I2	0.5	
13	**I2**	***Negative***		**Contact (via) between M2 and M3**
	13.1	I2 minimal size	1.8	
	13.2	I2 surrounded by M3	0.5	
14	**M3**	***Positive***		**M3 wiring layer**
	14.1	M3 minimal size	2.0	
	14.2	M3 minimal spacing	2.0	
	14.3	M3 minimal contact with R3	5.0	R3 layer is deposited directly on M3 (without insulation). To provide a reliable electrical contact between objects in R3 and M3 layers, the overlap should be no less than 5 micron.
15	**R3**	***Positive***		**Pd/Au contact metallization**
	15.1	R3 minimal size	5.0	
	15.2	R3 minimal spacing	3.0	
	15.3	R3 surrounded by M3	0.5	
16	**BMP**	***Positive***		**Cu/Au "bump" layer for MCM (optional)**
	16.1	BMP minimal size	30.0	
	16.2	BMP minimal spacing	50.0	

Planarized layers (6-layer process only)

1	**MN2**	***Positive***		**MN2 wiring layer**
	1.1	MN2 minimal size	0.8	
	1.2	MN2 minimal spacing	1.0	
	1.3	MN2 surround IN2	0.5	
2	**IN2**	***Negative***		**Contact (via) between MN2 and MN1**
	2.1	IN2 minimal size	1.0	
	2.2	IN2 surrounded by MN1	0.5	
3	**MN1**	***Positive***		**MN1 wiring layer**
	3.1	MN1 minimal size	0.8	
	3.2	MN1 minimal spacing	1.0	
	3.3	MN1 surround IN1	0.5	
4	**IN1**	***Negative***		**Contact (via) between MN1 and M0**
	4.1	IN1 minimal size	1.0	
	4.2	IN1 surrounded by MN1	0.5	
	4.3	IN1 spacing to M0	0.5	A via should always be covered with metal. M0 is a negative layer, -"spacing" instead of "surrounded by"
	4.4	IN1 edge spacing to J1	0.5	Crossing IN1 pattern with JJs is possible but not recommended

(1) The physical layer (metal or insulator) will be removed from the wafer in a filled area of a "negative" layer and will remain in a filled area of a "positive" layer.
(2) Rule "Layer A minimal size" means that linear size of an object in layer A should not be smaller than this in any direction.
(3) Rule "Layer A minimal spacing" means the minimal gap in layer A.
(4) Rule "Layer A spacing to layer B" means that an object in layer A should not be closer than this to any object in layer B (no overlap).
(5) Rule "Layer A edge spacing to layer B" means that edges of object in layer A should not be closer than this to any object in layer B. Note, that this rule allows object B being placed inside object A (but not vise versa).
(6) Rule "Layer A surrounded by layer B" means that an object in layer A should be placed inside object in layer B with at least this distance from its edges.
(7) Rule "Layer A surround layer B" means that an object in layer B should be placed inside object in layer A with at least this distance from its edges.

3.0 Physical Layer Process Specifications

3.1 Since the fabrication process involves projection photolithography and etching, the size of features (e.g., linewidth) on the wafer may systematically differ somewhat from the designed feature size. This change in size is called "bias". In the table below, the bias is defined as the shift of the object's edge due to its enlargement/reduction relative to its intended position in the design. It is often called single-side bias. A positive bias means that the digitized areas become larger on the wafer than in the design. The biases shown below for all layers, except J1/J2/J3, are applicable to relatively extended objects with sizes larger that the minimal feature size for a given layer. In most cases, sharp corners will be rounded up.

Layer	Material	Bias (3.1) μm	Physical layer properties: resistance, capacitance, *etc*.	Thickness nm
MN2	Nb	0.0±0.1	Nb, superconductor. Penetration depth λ_L = 80 nm ± 5%	200±20
IN2	SiO_2	0.0±0.1	SiO_2, insulator. Capacitance: 0.24 fF/μm² ± 20% or Si_3N_4, insulator. Capacitance: 0.4 fF/μm² ± 20%	200±40
MN1(3.6)	Nb	0.0±0.1	Nb, superconductor. Penetration depth λ_L = 80 nm ± 5%	200±20
IN1	SiO_2	0.0±0.1	SiO_2, insulator. Capacitance: 0.24 fF/μm² ± 20% or Si_3N_4, insulator. Capacitance: 0.4 fF/μm² ± 20%	200±40
M0(3.5)	Nb	0.0±0.1	Nb, superconductor. Penetration depth λ_L = 80 nm ± 5%	100±10/200±20
I0	SiO_2	0.0±0.1	SiO_2, insulator. Capacitance: 0.31 fF/μm² ± 10% or Si_3N_4, insulator. Capacitance: 0.53 fF/μm² ± 10%	150±15
M1	Nb	0.0±0.1	Trilayer base electrode, superconductor. λ_L = 100 nm ± 5%	135±10
J1/J2/J3	Nb	-0.08±0.02	Josephson tunnel junction counter electrode (see 3.2 and 3.3)	50±5
A1	Nb_2O_5/Al_2O_3	0.0±0.1	Layer of the anodized surface of the base electrode. Capacitance: 5.0 fF/μm² ± 20%	40±5
	SiO_2		SiO_2, insulator. Capacitance: 0.5 fF/μm² ± 10% or Si_3N_4, insulator. Capacitance: 0.8 fF/μm² ± 10%	100±10
R2	Mo	0.0 ± 0.1	2.1±0.3 Ohm per square (see table in 1.4)	40±6
	SiO_2		SiO_2, insulator. Capacitance: 0.5 fF/μm² ± 10% or Si_3N_4, insulator. Capacitance: 0.8 fF/μm² ± 10%	100±10
I1		0.0 ± 0.1	Contact hole through the above two SiO_2 layers	
M2	Nb	-0.1 ± 0.05	Nb, superconductor. Penetration depth λ_L = 80 nm ±5% ?	300±20
	SiO_2		SiO_2 insulator. Capacitance: 0.08 fF/μm² ± 10% or Si_3N_4, insulator. Capacitance: 0.13 fF/μm² ± 10%	500±40
I2		0.0 ± 0.1	Contact hole through the above insulator	
M3	Nb	-0.3 ± 0.1	Nb, superconductor. Penetration depth: λ_L = 80 nm ±5% ?	600±50
R3	Pd/Au	0.0 ± 1.0	Contact pads metallization	350±60
BMP	Cu/Au	0.0 ± 1.0	Layer for MCM bump	1500±100

3.2 We recommend using Josephson junctions of **circular** shape. The deviation of the radius of the circle in J1/J2/J3 layer is within +/- 20 nm. If such a deviation is critical, - use "digitized circular shape", i.e. a polygon with vertices of 135 degrees placed on 20-nm grid. Other shapes (square, octagon, etc.) can be used but Seeqc does not guarantee high accuracy of their area.

3.3 The dependence of JJ measured specific capacitance vs. critical current density of a Nb/AlOx/Nb trylayer can be approximated by the following function:

$$C_s = \frac{1000.0}{24.7 - 2.0 \cdot \ln j_c} \quad (fF/\mu m^2),$$

Here, C_s is the specific capacitance in fF/μm² and j_c is the critical current density in μA/μm², and plasma voltage in mV.

J_c (μA/μm²)	0.3	1.0	10.0	45.0	100.0	200.0
Cs (fF/μm²)	37	40	50	59	65	71
Vp (μV)	52	91	257	501	711	962

3.4 The critical current per micron width for Nb films is given in the following table

Nb Layer	MN2	MN1	M0[3.5]	M1	M2	M3
I_c **(mA/μm)**	40.0	40.0	20.0/40.0	30.0	50.0	70.0

If the wire crosses over steps, its I_c may drop by more than 50%. Please, see the minimal width of a wire in table 2.1 and its bias in table 3.0 before designing current transmitting lines.

3.5 Layer M0 in the 6-layer (planarized) process is twice thicker than in the standard 4-layer process.

3.6 At the request, MN1 layer can be a high-kinetic-inductance layer (HKIL) comprising a 40-nm NbNx film with 8.5-pH sheet inductance at 4.2 K.

4.0 Lithography features

4.1 Mask Grid Size

Layer	Polarity	Grid Size [μ]
MN2	Clear field	0.1
IN2	Clear field	0.1
MN1	Clear field	0.1
IN1	Clear field	0.1
M0	Dark field	0.1
I0	Dark field	0.1
M1	Clear field	0.1
J1	Clear field	0.02
J2	Clear field	0.02
A1	Clear field	0.1
R2	Clear field	0.1
I1	Dark field	0.1
M2	Clear field	0.1
I2	Dark field	0.1
M3	Clear field	0.1
R3	Dark field	0.1
BMP	Dark field	0.1

("Clear field" polarity means that the digitized area on the mask is covered with chrome).

4.2 Layers J1 and J2 have grid size of 20 nm. All remaining layers must use grid size of 100 nm. Every pixel coordinates are being rounded up to a multiple of grid.

4.3 All layouts will be printed on wafers as you see them on your computer screen (no mirroring).

5.0 Designs Submission Formats

5.1 The format of layout file is GDS-II.

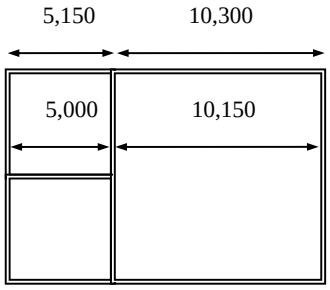
5.2 Please submit designs to Seeqc through File Transfer Protocol (FTP) at ftp://customer@ftp.seeqc.com or, if the size of the file is **less than 10 MB**, via E-mail to foundry@seeqc.com.

5.3 The active chip area for the design is limited to 5,000 μm x 5,000 μm. On the wafer, it will be surrounded by a dicing channel. Dicing channels between chips are 150 μm wide. No objects are allowed inside a dicing channel (extending beyond the 5,000 μm x 5,000 μm area).

5.4 It is also allowed to submit a 1-cm chip. In this case, the design area is 10,150 μm x 10,150 μm. No objects are allowed beyond the 10,150 μm x 10,150 μm area.

5.5 All other sizes should be negotiated with Seeqc prior the submission.

5.6 When delivering layouts of multiple chips to Seeqc, send only **one** GDS file, with all chips placed together in a single "supercell" on a **2,575-μm** grid. A chip insertion point should be at the geometrical center of the chip, i.e. – on the 2,575-μm grid



5.7 No cell (SREF) name may exceed **60 characters**. Cell names will be truncated to this size automatically and might clobber other cells.

5.8 We **do not support** GDS cell (SREF) placements that are rotated by a not multiple of **90 degrees** angle.

6.0 Cycle Time

6.1 Less than 2 months are required to process a standard (4-layer) wafer.

6.2 Less than 3 months are required to process an advanced (6-layer) wafer

6.5 Note: fabrication time may vary depending upon customer requirements.

6.6 On average, Seeqc has 6 releases per year. See www.Seeqc.com for up-to-date information and schedules.

7.0 Miscellaneous

- You must reserve your chip sites at least two weeks prior to the release date.
- Consult Seeqc and obtain an updated quote before submitting layouts.
- If you get permission to update the already-submitted layout, submit the revised layout without changing the names of the parent chips and/or the name of the main cell containing the parent chips. 5mm x 5mm or 10mm x 10mm chips are considered parent chips.
- If you need a layout example, send a request to foundry@seeqc.com
    - Layout of a junction defined using anodization.
    - Layout for a simple logic circuit.
    - Layout of a master cell.
- If you use logos or structures in your layouts that are not part of active circuits, make sure that they also follow design rules. We will reject layouts that contain excessive design rule violations.
- Do not “flatten” your chips, - we add specific prefixes to all cell names to prevent name conflicts.
- We fabricate and deliver from 4 to 16 copies of your chips (depending on reticle placement). Should you need specific number of copies, - please contact Seeqc prior the release.